

EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 01005070
PUBLICATION DATE : 10-01-89

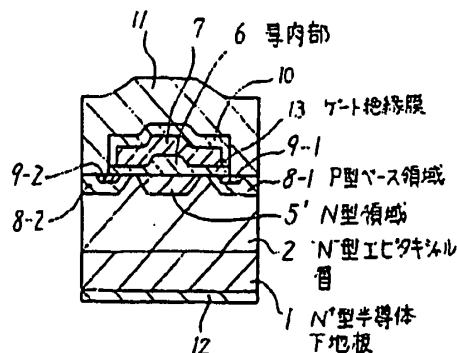
APPLICATION DATE : 26-06-87
APPLICATION NUMBER : 62160612

APPLICANT : NEC CORP;

INVENTOR : YAMAMOTO MASANORI;

INT.CL. : H01L 29/78

TITLE : VERTICAL INSULATED GATE FIELD
EFFECT TRANSISTOR



ABSTRACT : PURPOSE: To reduce an ON resistance and avoid punch through by a method wherein a thick part is provided at a part of a gate insulating film apart from base regions and a high impurity concentration region with a conductivity type same as that of a substrate is provided in the main surface of the substrate directly under the thick part of the gate insulating film.

CONSTITUTION: On the main surface of a substrate composed of an N-type semiconductor foundation board 1 made of silicon and an N-type epitaxial layer 2 built up on the foundation board 1, P-type base regions 8-1 and 8-2 are provided and, at the same time, a gate insulating film 13 is formed on the main surface of the substrate including the base regions 8-1 and 8-2. A thick part 6 is provided in the film 13 at the position apart from the regions 8-1 and 8-2 and, further, an N-type region 5' which has a higher impurity concentration than its surroundings is provided in the substrate directly under the thick part 6 apart from the regions 8-1 and 8-2. With this constitution, the spread of a depletion layer between the regions 8-1 and 8-2 and the substrate can be suppressed.

COPYRIGHT: (C)1989,JPO&Japio